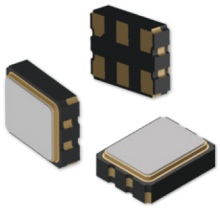
4.4 LV3225

3.2 x 2.5 mm SMD LVPECL/LVDS/ HCSL Crystal Oscillator



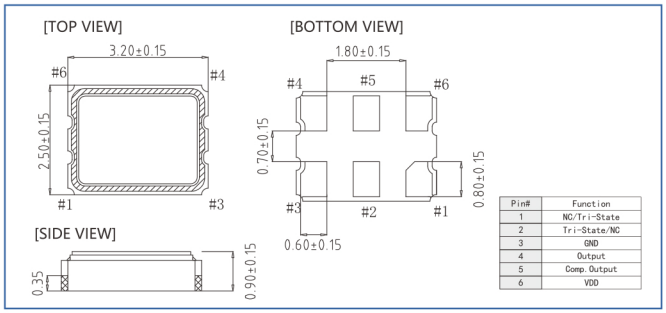
FEATURES

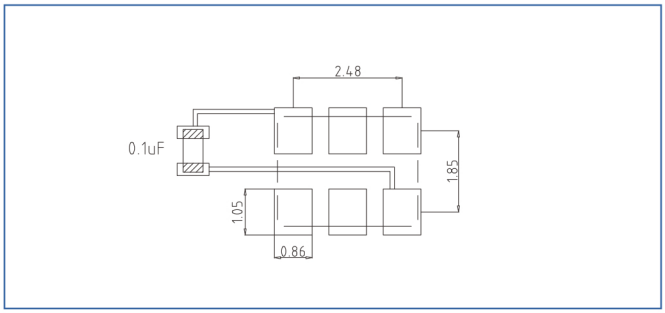
- Industry Standard 3.2 x 2.5 x 0.9 hermetically sealed ceramic package
- Very low jitter performance: typical 0.1 pS RMS from 12 kHz ~ 20 MHz
- Fundamental/3rd overtone crystal design
- Output frequency up to 250 MHz
- Tri-state enable/disable
- Up to 125°C operating temperature range

TYPICAL APPLICATION

- 10 Gbit Ethernet, Fiber Channel, Storage Area Network, SONET
- Enterprise Servers, Reference clocks for ADC and DAC
- Telecom

DIMENSIONS





ELECTRICAL SPECIFICATION

Parameter		LVPECL 3.3V Min.	LVPECL 3.3V Max.	LVPECL 2.5V Min.	LVPECL 2.5V Max.	LVDS 3.3V Min.	LVDS 3.3V Max.	LVDS 2.5V Min.	LVDS 2.5V Max.	Unit
Supply Voltage Variation (VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		10	250	10	250	10	250	10	250	MHz
Standard Frequency		25, 106.25, 125, 156.25, 161.1328, 212.5								
Supply Current	10MHz≤F_O<160MHz	—	75	—	75	—	50	—	50	mA
	160MHz≤F_O<250MHz	—	100	—	100	—	50	—	50	
Output Level	Output High	2.275	—	1.475	—	—	1.6	—	1.6	V
	Output Low	—	1.68	—	0.88	0.9	—	0.9	—	
Transition Time: Rise/Fall Time+		—	1	—	1	—	1	—	1	nSec
Startup Time		—	10	—	10	—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	2.31	—	1.75	—	2.31	—	1.75	—	V
	Disable (Low Voltage or GND)	—	0.99	—	0.75	—	0.99	—	0.75	
Aging (@25°C, 1st Year)		—	±3	—	±3	—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	-55	125	°C
Phase Noise @ 156.25 MHz	100 Hz	-95		-90		-90		-90		dBc/Hz
	1 kHz	-125		-125		-120		-120		
	10 kHz	-140		-140		-140		-140		
RMS Phase Jitter (Intergrated 12 KHz ~ 20MHz)	F_O<80MHz	—	1	—	1	—	1	—	1	pSec
	80MHz≤F_O<125MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	125MHz≤F_O<170MHz	—	0.3	—	0.3	—	0.3	—	0.3	
	170MHz≤F_O<200MHz	—	0.5	—	0.5	—	0.5	—	0.5	
	200MHz≤F_O	—	0.3	—	0.3	—	0.3	—	0.3	

Parameter		HCSL				Unit
		3.3V		2.5V		
		Min.	Max.	Min.	Max.	
Supply Voltage Variation(VDD)		VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range		25	175	25	175	MHz
Standard Frequency		100				
Supply Current	25MHz≤F_O≤175MHz	—	50	—	50	mA
Output Level	Output High	0.6	—	0.58	—	V
	Output Low	—	0.15	—	0.15	
Transition Time: Rise/Fall Time+		—	0.5	—	0.5	nSec
Startup Time		—	10	—	10	mSec
Tri-State (Input to Pin2 or Pin1)	Enable (High Voltage or Floating)	0.7VDD	—	0.7VDD	—	V
	Disable (Low Voltage or GND)	—	0.3VDD	—	0.3VDD	
Aging (@25°C, 1st Year)		—	±3	—	±3	ppm
Storage Temp. Range		-55	125	-55	125	°C
RMS Phase Jitter (Intergrated 12KHz ~ 20MHz)	25MHz≤F_O≤175MHz	—	0.5	—	0.5	pSec

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.
+ Transition times are measured between 20% and 80% of VDD.

FREQ. STABILITY vs. TEMP. RANGE

Temp.(°C) \ ppm	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	△	○
-40 ~ +125	×	○

*o: Available Δ: Condition X: Not available
*Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration.

Note: not all combination of options are available. Other specifications may be available upon request.
Specifications subject to change without notice.